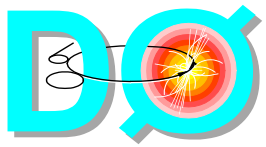
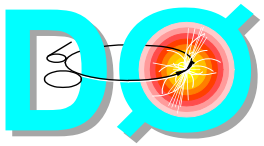
SVX4 Test Stand Update



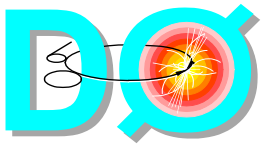
Testing Schemes

- LBL and William Wester wafer testing:
  - Level translation, UNIX based testing suite used by LBL for SVX3 testing, every mode of operation will be tested, and every capacitor in the pipeline will be tested extensively.
- Stimulus System:
  - Sophisticated pattern generator controlled by a PC, probe station, digital analysis system.

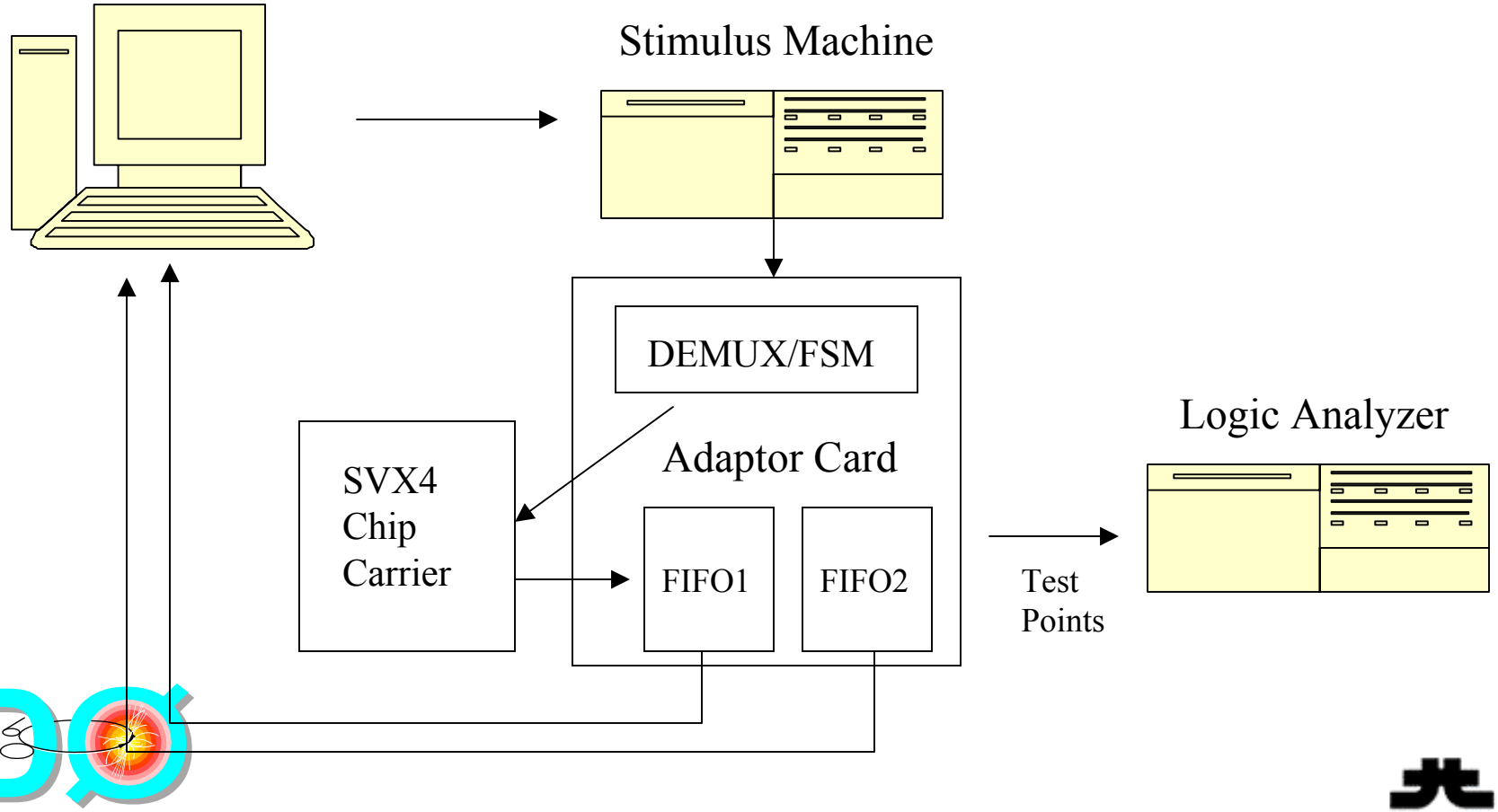


Stimulus System

- Does advanced scans: standard (pedestals), calibration (injection of charge), checks channel IDs, ramp pedestals, L1A delay scan, pipeline depth scan.
- Can be used to diagnose/repair detector components.
- System is capable of handling the readout of 14 chips (a.k.a. it can test hybrids).

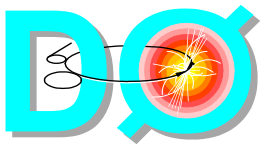


Schematic of Stimulus System



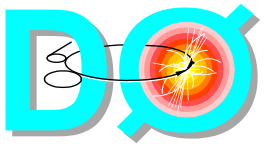
Timing Issues

- The Stimulus machine outputs a waveform to the board (vector format). This output has two clock signals: FE_CLK and BE_CLK.
- During digitization the BE_CLK operates at 53 MHz.
- During readout the BE_CLK operates at 26.5 MHz. The FIFO's are clocked at 26.5 MHz, but the first FIFO reads the high part of the clock and the second FIFO reads the low part of the clock, effectively reading out at 53 MHz.



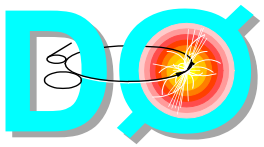
FIFO Issues

- In current design, the FIFO's are rated up to 40 MHz, but that gives 80 MHz data output rate in readout mode (51% deviation).
- Depth of the FIFOs is only 240 events, but as you add more chips this decreases by 240/n, where n is the number of chips.
- Plan to use 64K FIFOs instead of 32K FIFOs.



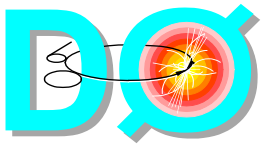
Altera Issues

- Old 5V chip: sources 4 mA
  sinks 12 mA
- New 2.5V chip: sources 1 mA
  sinks 2 mA
- 4 output lines feed LVDS driver and 4 outputs go directly across the board to the SVX chip. How many chips can the new chip drive?



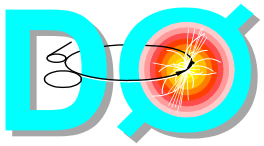
Recent News

- The test stand has been relocated in WH on the 14th floor. It has been reassembled and everything is working.
- Broken power supply has been fixed.
- John Ledford has the initial adaptor board schematic completed and is presently laying out the board.



Things to do

- Clear up some issues concerning grounding and power (top priority, i.e. talk to Marvin).
- Request a network connection to the test setup. I have already requested this, but I have to make sure that it has been done.
- Upgrade the computer. We have a computer ready to go, but we do not have the right compiler yet. We know who has it, we just have to get it.



Schedule

- Once grounding scheme is clear, final specs for board can be emailed out for D0 and CDF approval on Wednesday of this week.
- We can then give till next Monday for people to comment.
- Submit the design that same week (March 3rd -9th) and then it should take three weeks to get the boards back (submission is for the SVX4 adapter board and the SVX3 backward adaptor).